



T-45-19-05

## SP8685A&B

500MHz ÷ 10/11

The SP8685 is an ECL variable modulus divider, with ECL 10K compatible outputs. It divides by 10 when either of the ECL control inputs,  $\overline{PE1}$  or  $\overline{PE2}$ , is in the high state and by 11 when both are low (or open circuit).

### FEATURES

- Divides by 10 and 11
- AC Coupled Input (Internal Bias)
- ECL Compatible Output

### QUICK REFERENCE DATA

- Supply Voltage: -5.2V
- Power Consumption: 300mW
- Temperature Range:
  - 55°C to +125°C (A Grade)
  - 30°C to +70°C (B Grade)

### ABSOLUTE MAXIMUM RATINGS

Supply voltage	-8V
Output current	20mA
Storage temperature range	-55°C to +150°C
Max. junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p

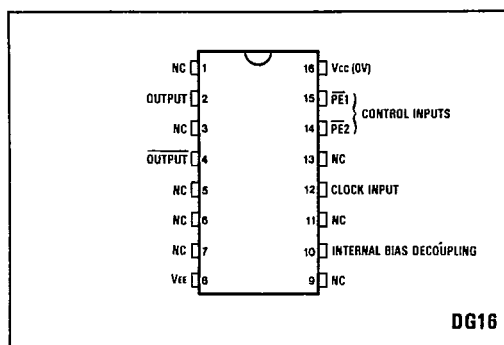


Fig.1 Pin connections - top view

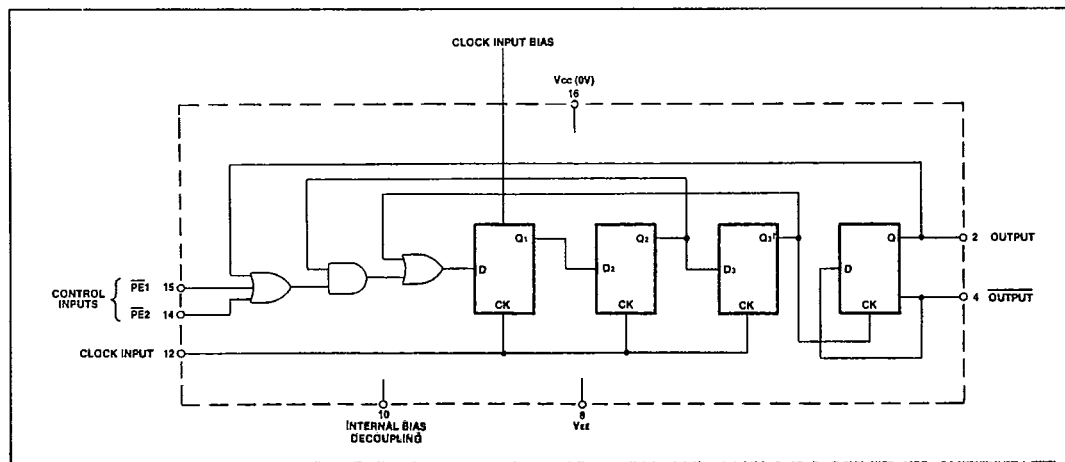


Fig.2 Functional diagram

# ELECTRICAL CHARACTERISTICS

Supply Voltage:  $V_{CC} = 0V$   $V_{EE} = -5.2V \pm 0.25V$   
 Temperature: A Grade  $T_{amb} = -55^{\circ}C$  to  $+125^{\circ}C$   
 B Grade  $T_{amb} = -30^{\circ}C$  to  $+70^{\circ}C$

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	$f_{max}$	500		MHz	Input = 400-800mV p-p	Note 6
Minimum frequency (sinewave input)	$f_{min}$		50	MHz	Input = 400-800mV p-p	
Power supply current	$I_{EE}$		70	mA	$V_{EE} = -5.2V$	Note 6
Output high voltage	$V_{OH}$	-0.87	-0.7	V	$V_{EE} = -5.2V$ (25°C)	
Output low voltage	$V_{OL}$	-1.8	-1.5	V	$V_{EE} = -5.2V$ (25°C)	
PE input high voltage	$V_{INH}$	-0.93		V	$V_{EE} = -5.2V$ (25°C)	
PE input low voltage	$V_{INL}$		-1.62	V	$V_{EE} = -5.2V$ (25°C)	
Clock to output delay	$t_p$		6	ns		Note 7
Set-up time	$t_s$	2		ns		Note 7
Release time	$t_r$	2		ns		Note 7

## NOTES

1. Unless otherwise stated, the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The temperature coefficient of  $V_{OH} = +1.63mV/^{\circ}C$ ,  $V_{OL} = +0.94mV/^{\circ}C$  and of  $V_{IN} = +1.22mV/^{\circ}C$  but these are not tested.
3. The test configuration for dynamic testing is shown in Fig.6.
4. The set up time  $t_s$  is defined as minimum time that can elapse between L  $\rightarrow$  H transition of control input and the next L  $\rightarrow$  H clock pulse transition to ensure that +10 is obtained.
5. The release time  $t_r$  is defined as the minimum time that can elapse between H  $\rightarrow$  L transition of the control input and the next L  $\rightarrow$  H clock pulse transition to ensure that the +11 mode is obtained.
6. Tested at 25°C only.
7. Guaranteed but not tested.

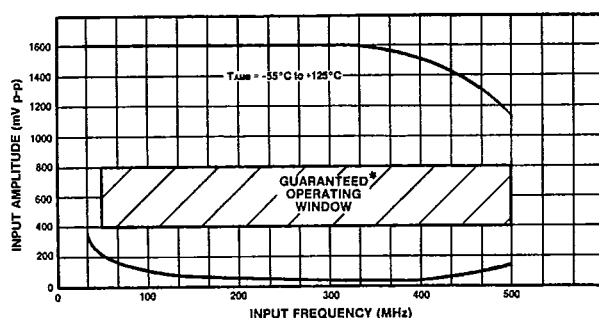


Fig.3 Typical input characteristic SP8685A

\*Tested as specified in table of Electrical Characteristics

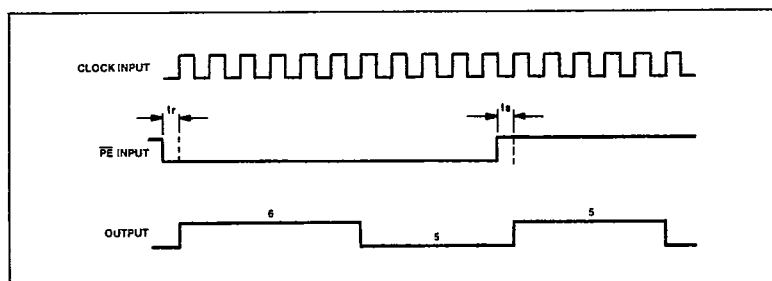


Fig.4 Timing diagram

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OPERATING NOTES

- 1. The clock input is biased internally and is coupled to the signal source with a suitable capacitor. The input signal path is completed by an input reference decoupling capacitor which is connected to earth.
- 2. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 15k resistor from clock input (Pin 12) to  $V_{EE}$ . This will reduce the input sensitivity by approximately 100mV.
- 3. The circuit will operate down to DC but slew rate must be better than 100V/ $\mu$ s.
- 4. The outputs are compatible with ECL II but can be interfaced to ECL 10K as shown in Fig.7.
- 5. The PE inputs are ECL III/10K compatible and include a 4.3k internal pulldown resistor. Unused inputs can therefore be left open.

TRUTH TABLE FOR CONTROL INPUTS

PE1	PE2	Division Ratio
L	L	11
H	L	10
L	H	10
H	H	10

- 6. Input impedance is a function of frequency. See Fig. 5.
- 7. All components should be suitable for the frequency in use.

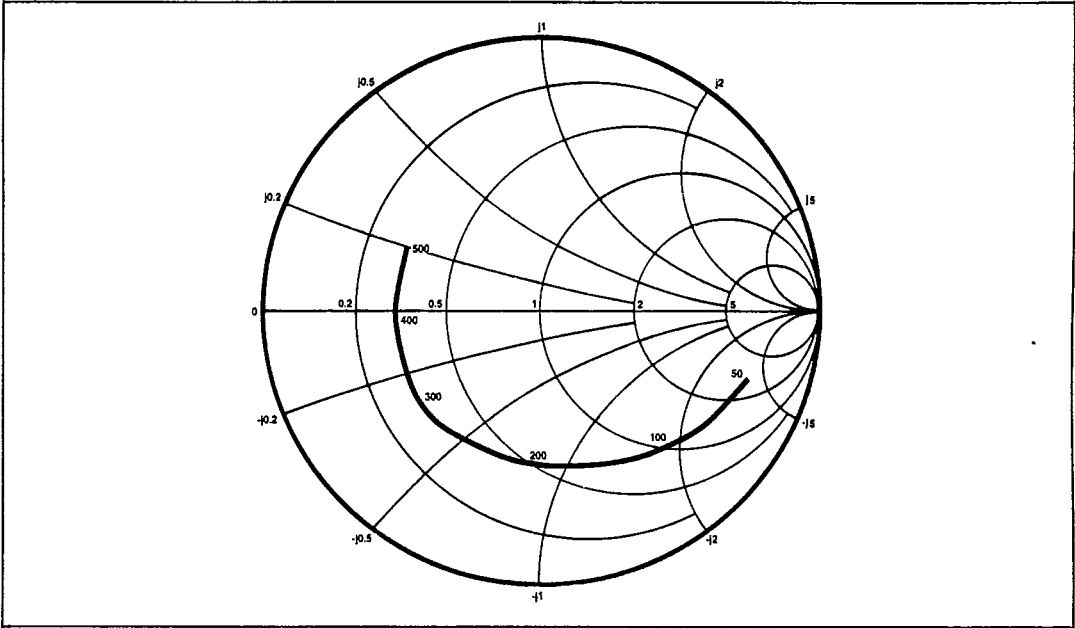


Fig.5 Typical input impedance. Test conditions: supply voltage -5.2V, ambient temperature 25°C, frequencies in MHz, impedances normalised to 50 ohms.

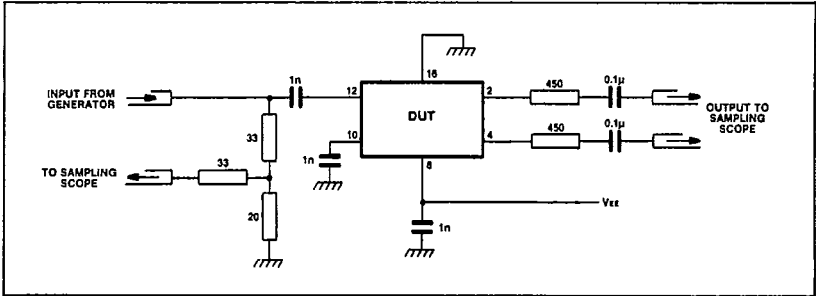


Fig.6 Test circuit

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PLESSEY SEMICONDUCTORS

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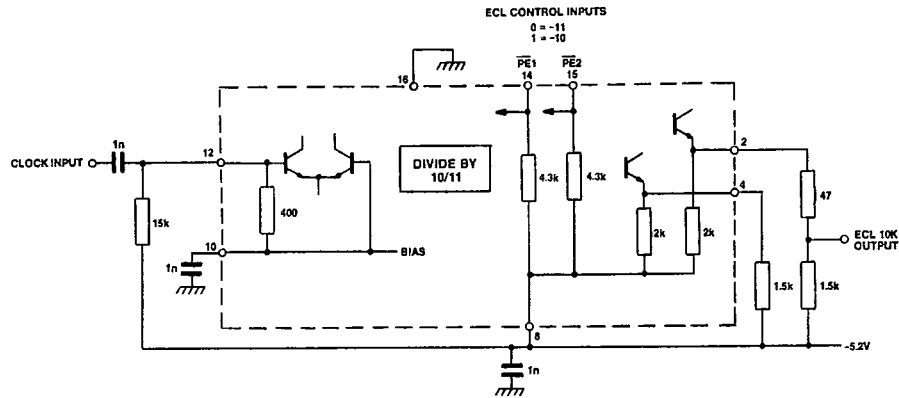


Fig.7 Typical application showing interfacing